

Serial No.:

FIS920030183US1

10/605,108

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

Applicant:

Dureseti Chidambarao, et al.

(Use several sheets if necessary)

Page 1 of 1

Filing Date:

September 9, 2003

Group:

2814

REFERENCE DESIGNATION

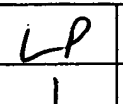
U.S. PATENT DOCUMENTS

EXAMINERS INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
		F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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DATE CONSIDERED

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FORM PTO-1449 (Modified)		ATTY. DOCKET NO. FIS920030183US1	SERIAL NO. 10/605,108
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
LP						
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
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	6,509,618 B2	1/21/03	Jan et al.			
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	6,362,082 B1	3/26/2002	Doyle et al.			
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	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
✓	6,506,652	01/14/03	Jan, et al.			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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	3,602,841	8/31/1971	McGroddy			
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	6,531,369	3/11/2003	Ozkan, et al.			
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	6,498,358	12/24/2002	Lach, et al.			
	6,493,497	12/10/2002	Ramdani, et al.			
	6,403,975	6/11/2002	Brunner, et al.			
	6,361,885	3/26/2002	Chou			
	6,255,169	7/3/2001	Li, et al.			
	6,246,095	6/12/2001	Brady, et al.			
	6,165,383	12/26/2000	Chou			
	6,133,071	10/17/2000	Nagai			
	6,046,464	4/4/2000	Schetzina			
	6,025,280	2/15/2000	Brady, et al.			

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LP	5,940,736	8/17/1999	Brady, et al.			
	5,880,040	3/9/1999	Sun, et al.			
	5,861,651	1/19/1999	Brasen, et al.			
	5,679,965	10/21/1997	Schetzina			
	5,670,798	9/23/1997	Schetzina			
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	5,108,843	4/28/1992	Ohtaka, et al.			
	5,060,030	10/22/1991	Hoke			
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	6,261,964	7/17/2001	Wu, et al.			
	6,221,735	4/24/2001	Manley, et al.			
	6,117,722	9/12/2000	Wuu, et al.			
	6,107,143	8/22/2000	Park, et al.			
	6,090,684	7/18/2000	Ishitsuka, et al.			
	6,066,545	5/23/2000	Doshi, et al.			
	6,008,126	12/28/1999	Leedy			
	5,946,559	8/31/1999	Leedy			
	5,840,593	11/24/1998	Leedy			
	5,592,018	1/7/1997	Leedy			
	5,592,007	1/7/1997	Leedy			
✓	5,571,741	11/5/1996	Leedy			

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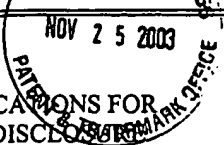
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	5,354,695	10/11/1994	Leedy			
	5,134,085	7/28/1992	Gilgen, et al.			
	5,006,913	4/9/1991	Sugahara, et al.			
	4,952,524	8/28/1990	Lee, et al.			
	4,855,245	8/8/1989	Neppl, et al.			

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LP	<p>Novel Locally Strained Channel Technique for High Performance 55 nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4 IEDM 27</p> <p>Local Mechanical-Stress Contro; (LMC): A New Technique for CMOS-Performance Enhancement A. Shimizum. et al. 2001 IEEE, 19.4.1-19.4.4 IEDM 01-433</p>
↓	<p>Mechanical Stress Effect of Etch-Stop Nitride and its impact on Deep Submicron Design Shinya Ito, et al. 2000 IEEE, 10.7.1-10.7.4 IEDM 00-247</p> <p>A Highly Dence, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications F. Ootsuka, et al. 2000 IEEE, 23.5.1-23.5.4 IEDM 00-575</p>

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